

# CALL FOR PAPERS

## International Workshop on RISC-V for HPC (RISCV-HPC)

Open Hardware, Open Possibilities –  
Advancing HPC with RISC-V

With HiPC 2025 | Hyderabad, India

December 17, 2025 (Half Day)

Workshop Info:  
[https://www.cdac.in/index.aspx?id=ev\\_HIPC](https://www.cdac.in/index.aspx?id=ev_HIPC)

A platform for researchers, developers, and application scientists to explore the impact of RISC-V in High-Performance Computing.

### WORKSHOP FOCUS

- ✓ RISC-V architecture innovations for HPC
- ✓ Compiler, runtime & toolchain development
- ✓ HPC application porting & benchmarking
- ✓ OS, virtualization, & resource management
- ✓ Accelerators, interconnects & co-design
- ✓ Exascale & heterogeneous HPC integration
- ✓ Security, reliability & resilience
- ✓ Community efforts & standardization

### SUBMISSIONS

Short Paper: 4 pages

Full Paper: 6–8 pages

Format: IEEE 2-column style

Review: Single-blind

Accepted papers → IEEE Xplore (HiPC  
companion proceedings)

### IMPORTANT DATE

|                     |               |               |               |               |
|---------------------|---------------|---------------|---------------|---------------|
| ●                   | ●             | ●             | ●             | ●             |
| SEPT 1, 2025        | OCT. 03, 2025 | NOV. 06, 2025 | NOV. 14, 2025 | DEC. 17, 2025 |
| Submissions<br>Open | Deadline      | Notification  | Camera Ready  | Workshop      |

### Organizers

- Sanjay Wandhekar, C-DAC, India
- Ashish Kuvelkar, C-DAC, India
- Yogeshwar Sonawane, C-DAC, India
- Nick Brown, EPCC, UK
- Teresa Cervero, BSC, Spain
- Surendra Billa, C-DAC, India

### SUBMISSION LINK



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conf=riscvhpc2025](https://easychair.org/conferences/conf=riscvhpc2025)

For More Information, Contact: [riscvhpc2025\[at\]cdac\[dot\]in](mailto:riscvhpc2025[at]cdac[dot]in)