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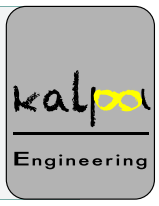

Realization of Active Neutral Point Clamp Multilevel Inverter Using SPWM Technique

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Abstract

Because of some technical and some historical reasons AC power is more popular than DC. Inverter has become very important power electronics converter for having adjustable AC power output which is need of majority of industrial equipments. For better quality of output various modulation techniques are being implemented. As these techniques require high frequency operation which results in higher switching losses multilevel inverter are preferred for medium and high power applications. Multilevel inverters can give better quality output at low modulating frequency because of their multi step output. In this paper popular Sine wave Pulse Width Modulation (SPWM) has been implemented for Active Neutral Point Clamp (ANPC) multilevel inverter which has some better features with respect to standard diode clamp, flying capacitor or cascaded H-bridge topologies. This kind of multilevel inverter is a hybrid type of multilevel inverter in which a 3 level flying capacitor clamp multilevel inverter is cascaded to a 3 level diode clamp multilevel inverter. As low frequency Selective Harmonic Elimination technique has limitation of computational complexity for elimination of more than two harmonics simultaneously SPWM has been implemented to achieve a good quality output. Advance Risk Machine (ARM) controller has been used for generating control signals. Complete scheme has been discussed in this paper. Prototype of 5 level ANPC has been fabricated for experimentation and results are presented from the experiments.

1 Introduction

In this work a prototype of single phase of 5 level Active Neutral Point Clamp Multilevel Inverter has been prepared. Then with the help of advance 32-bit microcontroller Sine PWM has been implemented and controlling pulses are made available. With suitable driver circuits the power

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switches are triggered and outputs are recorded in CRO for further analysis. Complete work has been divided in three parts. First is "Introduction to Active Neutral Point Clamp Multilevel Inverter". Second is "Modified carrier based Sine PWM for Multilevel Inverter". Third is Implementation and Results. Introduction to active neutral point clamp multilevel inverter

There are three basic topologies for multilevel inverter: Diode clamp or NPC, Flying capacitor, Cascaed H-bridge. All have their merits and demerits for various aspects. Researchers are trying to derive better topologies by combining merits of basic topologies. Active Neutral Point Clamp is one of such topology. It requires less count of devices for same level of output in comparison to basic three topologies. Also it does not require isolated DC supplies as in cascaded H-bridge topology.[1,4] Figure-1 shows basic scheme for deriving 5 level output from DC link.

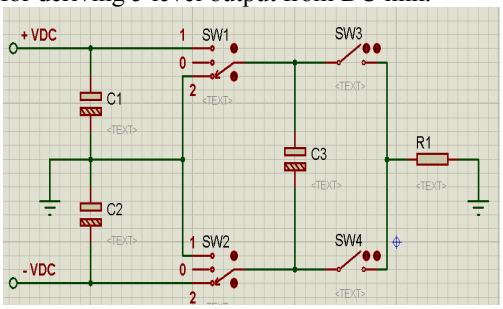

Figure 1.Scheme for five level output

DC link voltage V_{DC} is divided by two i.e. V_{DC} /2 with the help of two DC link capacitors C1 and C2. SW1 and SW2 are two Three-way switches. SW3 and SW4 are two SPST switches. C3 is floating capacitor. R1 is load to the inverter. If SW1 is at '1' and SW3 is close Vout will be V_{DC} /2 with respect to neutral point. Likewise if SW2 is at 2 and SW4 is close Vout will be – V_{DC} /2. If SW1 is at 2 and SW3 is closed Vout will be 0. Same way if SW2 is at 1 and SW4 is closed Vout will be 0. There is redundancy for 0 V output. But it is not of much use. There is interesting and very useful redundancy for Vout = ± V_{DC} /4. We can get + V_{DC} /4 output by (a) SW1 at '1' and SW4 is close or (b) SW2 at 1 and SW3 is close. Same way we can get – V_{DC} /4 output by (a) SW2 at 2 and SW3 is close or (b) SW1 at 2 and SW4 is close. For the cases 'a' floating capacitor C3 either charges or discharges giving same output level for respective 'b' cases. These redundancies can be used to maintain the charge on capacitor. This basic scheme is converted to actual power circuit in Figure-2. Eight power switches are required with reverse conducting diodes for reverse power flow capability. From all combinations of all 8 switches some are forbidden.

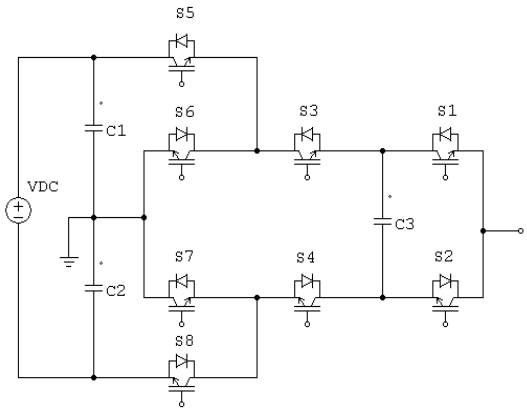

Figure – 2 Five level ANPC topology

Effectively eight switching combinations are utilized for achieving five level output shown in Figure-3.

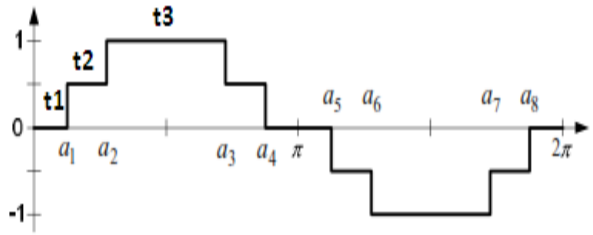

Figure 3. Output of five level inverter

Switches S1 & S2, S3 & S4, S5 & S6, and S7 & S8 are always operated in complementary fashion. Otherwise they will create shoot through fault in inverter. Moreover S5 & S7 and S6 & S8 operate simultaneously. By this we will require three switch control signals: one for S1 & S2 named G1, one for S3 & S4 named G2, one for S5, S6, S7 & S8 named G3. This reduces the complexity in control strategy. With three control signals we can have eight possible combinations.[2]

All this possibilities are called individual switching states. Table-1 gives details of all possible states of the configuration.

Table - 1

G3'	G3	G3'	G3	G2'	G2	G1'	G1		
S8	S7	S6	S5	S4	S3	S2	S1	V_{ph}	State
1	0	1	0	1	0	1	0	$-V_{dc}/2$	V1
1	0	1	0	1	0	0	1	$-V_{dc}/4$	V2
1	0	1	0	0	1	1	0	$-V_{dc}/4$	V3
1	0	1	0	0	1	0	1	0	V4
0	1	0	1	1	0	1	0	0	V5
0	1	0	1	1	0	0	1	$+V_{dc}/4$	V6
0	1	0	1	0	1	1	0	$+V_{dc}/4$	V7
0	1	0	1	0	1	0	1	$+V_{dc}/2$	V8

For better output quality and also for control we use various modulation techniques. If Selective Harmonic Elimination is used we have two switching angles for eliminating two harmonics simultaneously.[5] Which would give THD of around 17%.[7]. Another way is to implement optimized pulse pattern for Selective Harmonic Elimination.[3] For further improvement modified carrier based Sine Pulse Width Modulation is used.

2 Modified carrier based SPWM

In this method phase shifted or level shifted high frequency triangular waveforms are compared with low frequency modulating signal.[6]

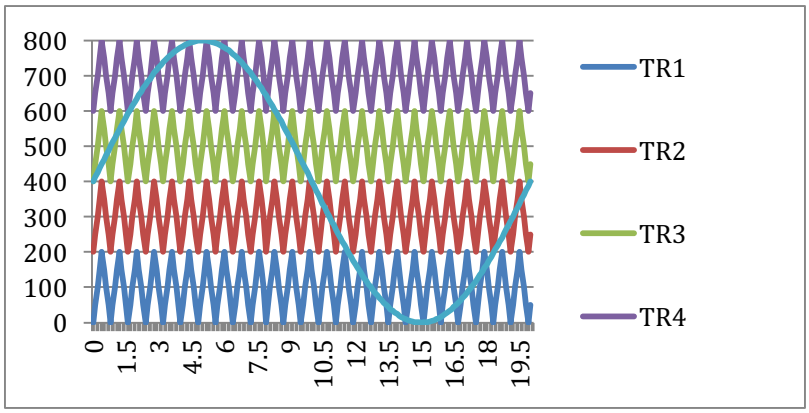

Figure -4 Modified carrier based SPWM

TR1, TR2, TR3, TR4 are high frequency (ten times or higher than modulating wave frequency) triangular waveforms. Which are one by one at a time are compared with modulating sine wave. This comparison will give required output level, not exact gating signals. This output is shown in Figure – 5.

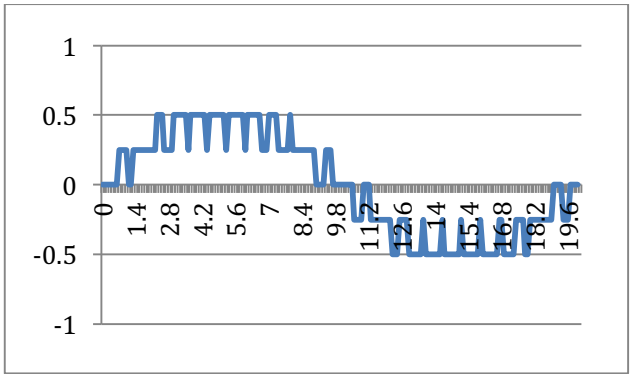

Figure – 5 Output of 5 level ANPC inverter

For this output to be generated by ANPC inverter shown in Figure-2, respective switching states from Table-1 is to be selected for particular output level. But when $\pm V_{DC}/4$ is the required output level, two redundancies are available. Real time floating capacitor voltage level is sensed and one of the switching states is to be selected which tends to maintain the charge on capacitor.

3 Implementation and results

For As higher computational speed is required for generating gating signals ARM microcontroller has been used. Four triangular waveforms and a modulating sinusoidal waveform has been generated digitally by equation set 1.

- TR1=Tringle[0]+Vmtr/(Ttr/2)
- TR2=Tringle[1]+Vmtr/(Ttr/2)
- TR3=Tringle[2]+Vmtr/(Ttr/2)
- TR4=Tringle[3]+Vmtr/(Ttr/2)
- Y=Vm * (1 + MI*(sin((6.283*SineIndex)/Tsine)))…1

One by one these triangle wave is compared with modulating signal to generate gating signals.[6] One period of modulating signal is divided in six sections.

- Section-1: Y < 600 : Gate pulse is derived by comparison of TR3 and Y
- Section-2: Y > 600 : Gate pulse is derived by comparison of TR4 and Y
- Section-3: Y > 400 : Gate pulse is derived by comparison of TR3 and Y
- Section-4: Y > 200 : Gate pulse is derived by comparison of TR2 and Y
- Section-5: Y < 200 : Gate pulse is derived by comparison of TR1 and Y
- Section-6: Y < 400 : Gate pulse is derived by comparison of TR2 and Y

Addition to above logic charge on capacitor is sensed to select particular output state and required switching signal. This complete scheme has been converted to embedded C program and loaded to STM32F4 ARM microcontroller. The control signals from controller are given to appropriate driver circuit which are fabricated by TLP250 totem-pole output driver IC. Finally driver circuit output are used to drive the power switches i.e. MOSFET IRF 540. Simulated control signals from uVision Keil software are shown in Figure-6.

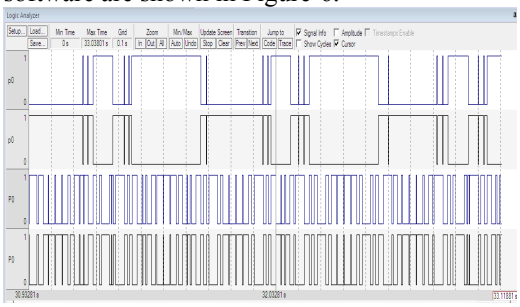

Figure – 6. Gate pulses G1 to G4.

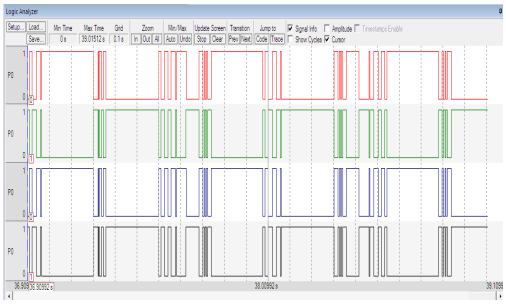

Figure – 7. Gate pulses G5 to G8.

TLP 250 IC is used for driver circuit fabrication. This IC gives totem-pole output which improves turn-on and turn-off characteristics of switching devices. MOSFET IRF 540 is used as power devices. Figure 8 shows pictorial view of prototype. After experimentation some outputs are recorded in oscilloscope. Figure –9 shows one of the recorded result.

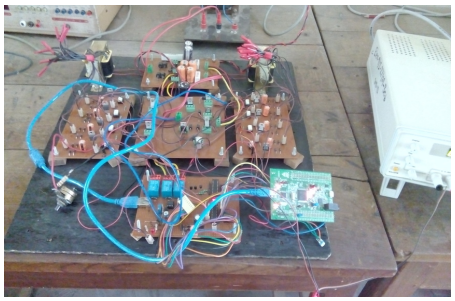

Figure-8 Hardware Prototype

Figure –9 Output of SPWM on ANPC inverter.

For Vin= 55V r.m.s., output frequency = 50 Hz Table – 2 gives some calculated parameters for the scheme.

Table 2

Vr.m.s.= 28.2814	V_{DC}= 77.7817

Vn r.m.s.		HFn	
1st	13.8185	HF_1	1
3rd	0.247228	HF_3	0.017891
5th	-0.17441	HF_5	-0.01262
7th	0.228811	HF_7	0.016558
9th	0.047643	HF_9	0.003448
11th	-0.0442	HF_{11}	-0.0032
13th	0.364128	HF_{13}	0.026351
15th	-0.6172	HF_{15}	-0.04466
THD = 21.71		DF= 0.97724	

These results are calculated. Verification with experimental results are in process.

4 Conclusion

From the reference of output waveform and calculated values, it seems to be a reasonably fair output of inverter which gives better quality output with medium switching frequency. And multilevel topology also helps to reduce switching device ratings.

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