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A Wide Bandwidth, Low Power, Linear Quantized-Analog VGA in 28 nm CMOS Technology and 1.2V Supply

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***Abstract*—This work presents wide-band/wide range Variable Gain Amplifier (VGA) based on the Quantized-Analog (QA) processing. The VGA is formed by an array of sub-units that amplify different portions of the input signal. The gain variation is obtained by acting on the signal correlation among adjacent slices that are eventually recombined on an output load. The VGA has been characterized, by inserting the VGA inside an optical RF front-end which includes a TIA stage and output buffer. Designed and layouted in 28nm CMOS, the VGA shows a gain variation of about 22 dB obtained in one stage, and a -3dB bandwidth of 29 GHz. At maximum gain, the average equivalent input-referred current noise is equal to 10.3 pA/$\sqrt{Hz}$ while the Total Harmonic Distortion (THD) is below 2.3% for a maximum output swing of 500-mV peak-to-peak differential. The VGA consumes 64 mW while the complete front-end 124 mW from a 1.2V voltage supply.**

***Index Terms*—wide-band, wide range, Variable Gain Amplifier, Quantized Analog (QA), optical RF front-end, signal correlation, gain variation, THD, and Equivalent Input referred current Noise.**

I. Introduction

The Variable Gain Amplifier represents a key block inside the receiver chain of wireline systems. It is used to provide a full-scale signal at the input of the ADC, allowing a conversion at a maximum signal-to-Noise Ratio. Therefore, a VGA is required in the circuits to maximize the dynamic range of the base-band signal. In the literature, most of the VGA stages for wide-band RF front-end are based on current steering [1], [2], [3] or Gilbert cell [4], [5] topology, where the gain is varied by controlling the subtraction ratio of the direct and the crossed-over current, flowing in the output load with a control voltage applied to the differential pairs. The main limitations of these architectures are the higher supply to provide sufficient voltage headroom for the cascode structure [6] and the limited input/output dynamic range, which leads to a lower voltage efficiency, $\eta_v[\%] = V_{out}/V_{DD}*100$, defined as the ratio of the maximum output swing and the voltage supply. In such topology, the ultimate limit to the gain variation is the dynamic range of the input stages which is typically limited (especially in current steering typologies). Hence, when a wide gain variation is required, multiple stages are necessary to guarantee a low distortion. The drawbacks of multiple stages are the higher power consumption and larger chip area (since more inductors are needed for bandwidth extension). This work aims to overcome the above limitations by implementing a wide-range gain variation in a single-stage amplifier by exploiting the proprieties of Quantize-Analog (QA) signal processing introduced in [7]. As shown in Fig 1, in the QA signal processing, the input voltage is sliced and amplified by an array of amplifiers. Such signal decomposition is obtained by applying at the input of each amplifier a different DC offset to shift the input-output transfer characteristic. Eventually, the

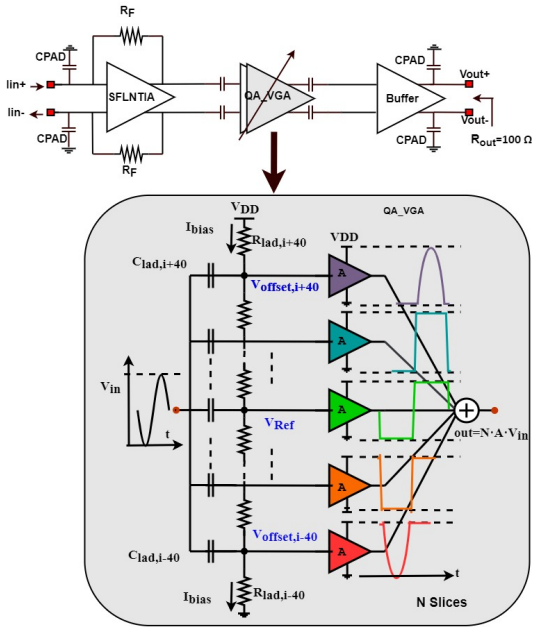

Fig. 1. Block Diagram of the proposed optical RF front-end with the QA-VGA Stage.

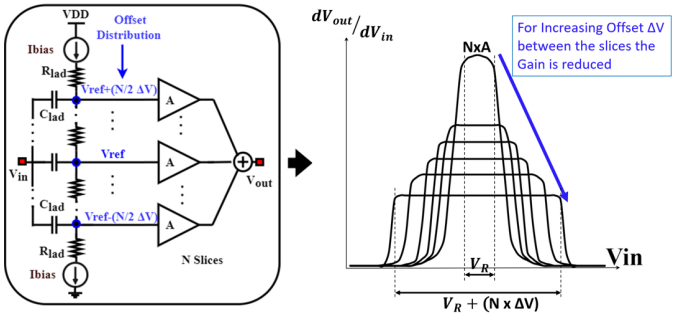

Fig. 2. Quantized Analog gain variation

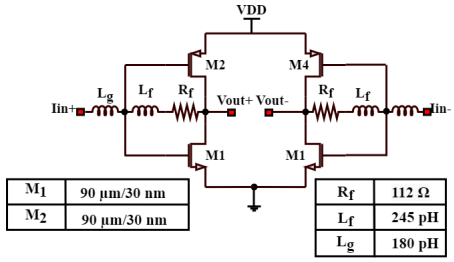

Fig. 3. Inverter-based shunt feedback Low Noise TIA (SFLNTIA)

processed signal is linearly recombined by summing all the different outputs. The gain variability is obtained by changing the signal correlation among the different slices through the DC offset distribution. The key feature of the use of the QA signal processing is an expansion of the input dynamic range when the gain is decreased (i.e. when the input signal is larger). This allows to overcome the limits of the classical topology, by allowing to reach a wide range gain variation while keeping a low distortion. By using a single stage to implement all gain variability in the chain, it is possible at the same time to reduce the power consumption, the number of inductors, and the complexity of the design. Fig.1 shows the overall system architecture of the RF Optical front-end including the proposed QA-VGA stage. The paper is structured as follows: Section II describes the QA-VGA and its gain variation, Section III details the design and architecture of the full front-end, Section IV provides post-layout simulation results, and Section V concludes the paper.

II. Quantized Analog Variable Gain Amplifier

The QA-VGA is an analog circuit that provides a tunable gain amplification based on Quantized Analog (QA) signal processing. In the QA structure, as displayed in Fig 2, an array of N amplifiers are used to slice the input signal. Each one of these amplifiers (or slices) has a gain of A and is biased with different DC voltages, in particular, the central slice is biased with a fixed voltage, while, an offset is applied to the slices above and below in a symmetrical way through a resistive ladder. The gain of the QA Amplifier depends only on the unsaturated slices [7], and it is regulated with the offset voltage (ΔV).

As shown in Fig2, by increasing ΔV, the gain decreases, and the input dynamic range increases. When ΔV is equal to 0 all the slices are overlapped, and the input range of the entire QA amplifier becomes equal to V_R (i.e input range of one amplifier) while the total gain after recombination is NxA, that is the maximum gain of the QA amplifier. If a generic offset ΔV is applied, the input range becomes $V_R + (N \cdot \Delta V)$. When the offset ΔV is equal to V_R, the input dynamic range is maximized and the total gain of the QA Amplifier is A, this is considered to be the minimum achievable gain.

III. Design and Architecture

The optical RF front-end consists of three stages ac-coupled, shown in Fig.1: an SFLNTIA which provides a fixed trans-impedance gain of 47 dBΩ, a QA-VGA (gain variation from 17 dB to -5 dB), and an output buffer terminated on a 100 Ω.

A. Shunt Feedback Low Noise Amplifier TIA (SFLNTIA)

The first stage of the receiver (SFLNTIA) is the trans-impedance amplifier that converts and amplifies the input current into a voltage. As shown in Fig 3, an Inverter-based shunt feedback TIA has been used, because of its better performance in terms of noise. It provides a fixed gain of 47 dBΩ (224 Ω). The feedback path is made of a fixed resistor,R_f, and the inductor, L_f, that is used to boost the gain at high frequency. Another input inductor, L_g is included to resonate out the input gate capacitance to further extend the bandwidth.

B. QA-VGA circuit

The QA-VGA is used in the receiver chain to provide gain variation and linearity compensation of the signal. The transistor-level circuit is shown in Fig. 4. It is formed by two CMOS amplifiers sliced into N units with a size of W/N, where W is the total width of the QA amplifier and N is the number of slices (81 in this case). The first stage inverter is used to slice the input signal and its gain is reduced with a dumping differential resistor $R_{int,i}$, in order to move the pole at a higher frequency and preserve the bandwidth. The second stage inverter is used to recombine the signal processed by each slice on the output differential resistor R_{out}. Also here inductive peaking both at the input and output node, has been exploited to enhance the bandwidth. A ladder of variable resistors, R_{Lad}, is used to generate the reconfigurable offset distribution, $V_{offset,i}$, among the slices. As shown in Fig. 5, each single resistor R_{Lad} is a series of 5 binary weighted resistors that can be shorted out using CMOS pass-gates placed in parallel, that are controlled with digital bits. As a result, different values of equivalent resistors for each slice can be achieved. By changing the value of the bias current flowing in the resistive ladder, it is possible to reduce or increase the relative offset between adjacent slices ($V_{offset,i}$) and with it their correlation toward the input signal. The QA-VGA provides a total gain variation of about 22 dB (from 17 dB to -5 dB). The maximum gain is reached when no offset is applied

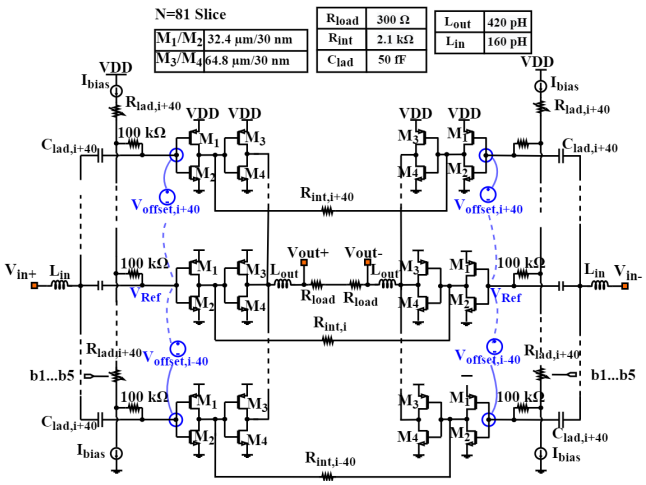

Fig. 4. Transistor Level Schematic of the differential QA-VGA.

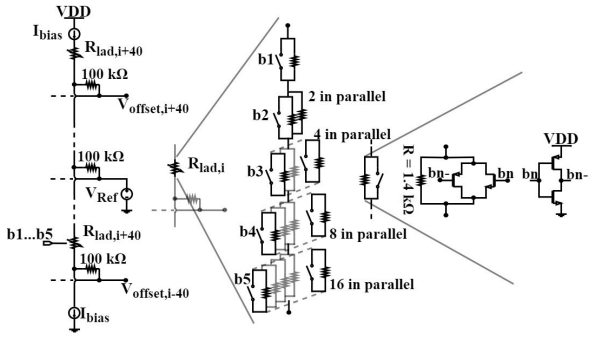

Fig. 5. Resistive ladder.

and the slices are all in parallel, while a minimum gain is obtained by increasing the offset and reducing the correlation between the slices.

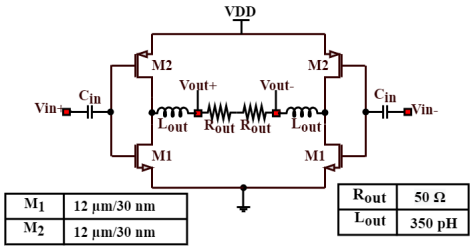

Fig. 6. Output Buffer.

C. Output Buffer

The last stage of the receiver chain is the output buffer shown in Fig. 6. It is an inverting stage ac-coupled with the QA-VGA, with a 100 Ω resistive termination and output inductor, L_{out}, for bandwidth extension. This stage buffers the signal processed by the previous circuits on the output pads of the chip.

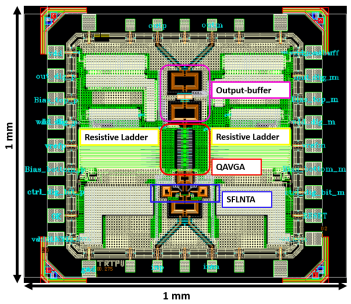

Fig. 7. Layout of the optical RF front-end .

IV. Post-Layout Simulation Results

The chip prototype has been implemented in TSMC 28-nm CMOS. Fig. 7 shows the layout of the optical RF front-end with a total size of 1mmx1mm including the input/output pads. All the reported results have been achieved from post-layout simulations. The target of this work is to have a maximum output swing of 500 mVppdiff (voltage peak to peak differential), with low noise and a THD always lower than 3% over the whole dynamic range of interest. As shown in the transfer function of the receiver in Fig. 8, a gain variation of 22 dB is obtained with the single-stage QA-VGA, by increasing the voltage offset, ΔV, between the adjacent slices. The maximum gain is 64 dBΩ with a bandwidth of 29 GHz (zero offsets, ΔV=0, all slices are overlapped), and the minimum gain is 42 dBΩ with a bandwidth of 30 GHz (ΔV=10 mV). The THD is always lower than 2.3 % for all the gain configurations, as shown in Fig.9. As it can be seen in Fig.10, the QA-VGA is able to provide an output swing of 500 mVppdiff with low distortion, despite the fact that it receives at the input a signal, coming from the SFLNTIA, that can go up to 880 mVppdiff. By integrating the output noise in the signal bandwidth and referring it to the input, the total average input-referred current noise of the receiver, as reported in Fig.11.a, is 10.3 pA/$\sqrt{Hz}$ in the worst case of maximum gain configuration, when the input signal is minimum. As shown in Fig.11.b most of the noise in this gain configuration is generated by the first stage SFLNTIA, while the contribution of the QAVGA is about 17.5%. The maximum dynamic power consumption of the receiver is 124 mW. Table I shows a comparison with the state of the art. Considering the CMOS and BiCMOS implementation, this work shows better results in terms of voltage efficiency (η_v= 42%), linearity, power consumption, and noise performance from a lower supply voltage of 1.2 V.

V. Conclusion

The proposed QA-VGA represents a good alternative to the standard topology, as a fully CMOS continuous VGA with low supply and power consumption, which can enable a higher level of integration and reduce the cost of the overall receiver system.

TABLE I
PERFORMANCE AND COMPARISON WITH THE STATE OF ART

	This Work*	[4]	[5]	[8]	[1]	[2]	[3]
Technology	28 nm CMOS	28 nm CMOS	28 nm CMOS	16 nm FinFET	130 nm BiCMOS	130 nm BiCMOS	130 nm BiCMOS
SE/S2D/Diff.	Diff	S2D	Diff	S2D	Diff	Diff	Diff
Gain@1GHz (dBΩ)	64	65	78	78	65	80	73
Gain variability (dB)	22	17	42	21	15	30	43
N° stage for gain Variation	1	3	4	4	1	2	2
Gain Control Type	QA Analog	Analog	Analog	Digital PGA	Analog	Analog	Analog
Supply (V)	1.2	2.5/1.2	2.4	1.8	3.3	3.3	3.3
Diff. Out Swing V_{out}(mV)	500	300	500	600	800	900	500
Voltage Efficiency η_v[%]**	42 %	12 %	21 %	33 %	24 %	27 %	15 %
THD (%)	<2.3% (@1GHz, 500 mV_{ppd})	<5% (@1GHz, 300 mV_{ppd})	1.77%(@1GHz, 500 mV_{ppd})	1.8%(@1GHz, 600 mV_{ppd})	<5%(@1GHz, 800 mV_{ppd})	4.13%(@1GHz, 900 mV_{ppd})	1.5%(@1GHz, 500 mV_{ppd})
Bandwidth (GHz)	29	60	42	27	66	53	27
Noise (pA/$\sqrt{Hz}$)	10.3	19.3	18	16.7	7.6	25	20
Power (mW)	124***	107	319	60.8	150	277	313

*Post-Layout Simulation Results.
**Voltage efficiency $\eta_v[\%] = (V_{out}/V_{DD}) * 100$
***Dynamic Power Consumption.

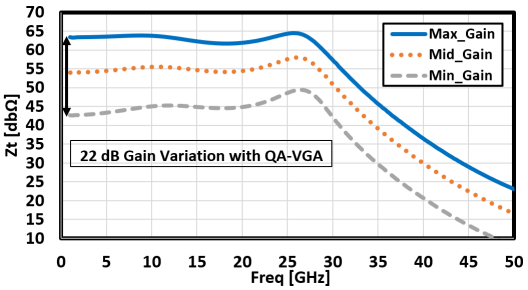

Fig. 8. Simulated transfer function of the receiver for three different gain configurations of the QA-VGA, maximum, medium, and minimum.

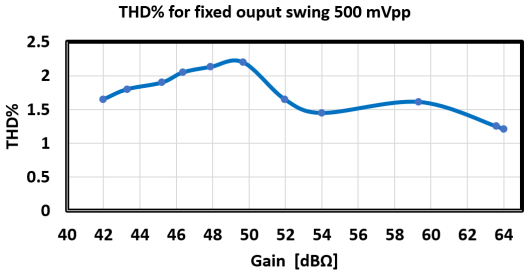

Fig. 9. Simulated THD over different gain settings for a fixed output swing of 500 mVpp.

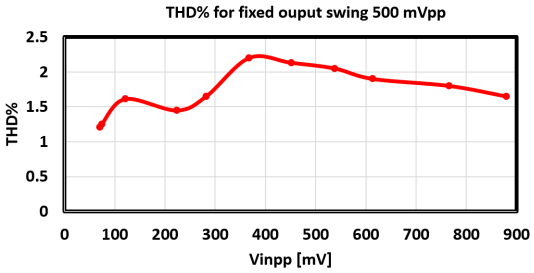

Fig. 10. Simulated THD for different values of input voltage swings (peak-to-peak diff.) of the QA-VGA keeping the output swing fixed at 500 mVpp.

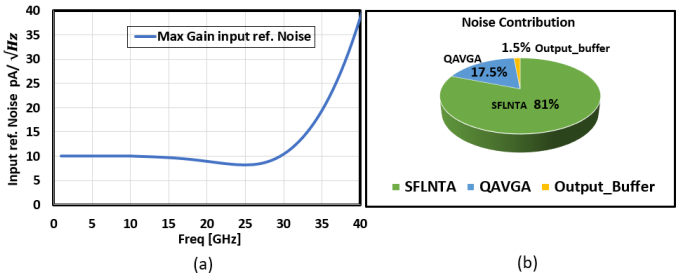

Fig. 11. (a) Equivalent input-referred current Noise. (b) Noise contribution of the different stages inside the receiver.

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