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Modeling and Design of the Inner Control Law of a Three-Phase Grid-Forming Inverter Operating Under the Droop Strategy ⋆

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Abstract: This work aims to design the internal control loop of a grid-forming converter, as well as demonstrate the stability of the system through the eigenvalues of the state space equation of the complete system. The developed method consists of designing the control loops separately, taking into account the influence of the PWM, the dynamics of the current control for the design of the voltage loop, that is, without using simplifications in the design that can lead the system to instability. The analysis of the performance of the designed system is done using simulation tools such as: Matlab/Simulink and the real-time simulation platform OP4500 in Hardware in the loop to verify if the system is stable and if it is capable of tracking the imposed references. The results obtained make it clear that the designed system is stable observing the eigenvalues obtained from the complete system and also by simulation that analyzes if the controllers are capable of tracking the references. In addition, the behavior of the system in steady state is analyzed to verify if the system is in fact stable. Therefore, the present work fulfills the objective of developing a method for calculating the internal network gains of the network-forming converter and ensuring the stability of the system through the state space equation and simulation of the complete system.

Keywords: Modeling; Grid-forming; Inner-loop; Power System; Droop;

1. INTRODUCTION

In recent decades, the global energy system has undergone a significant transformation, moving from a predominance of non-renewable energy sources to a greater penetration of renewable energy sources. This energy transition has led to a diversification of the energy mix, as well as a reduction in greenhouse gas emissions associated with energy production. These renewable sources are usually interfaced with the power grid through voltage source inverters, whose inertial response and damping are not provided naturally. In addition, the stability of the power grid and stand-alone microgrids is affected by power electronics-based generators (Kerdphol et al. (2021)). In this context, this increase in the number of static converters connected to the grid causes a decline in system inertia, causing a variation in the grid frequency that can lead to system instability (Tielens and Van Hertem (2016)).

There are two operating modes for voltage source converters, grid-following converters and grid-forming converters (GFMC), respectively. GFLC converters inject power into the grid by controlling the converter's output current (Bouzid et al. (2015)). In general, the GFLC converter needs a phase-look-loop (PLL) to follow the phase angle of a voltage at the point of common coupling (Wang et al. (2021)). As an alternative, GFMCs are emerging as a new trend (Lasseter et al. (2019)). GFMCs mimic the synchronization characteristics of synchronous generators and determine the desired voltage amplitude and phase at the point of common coupling, without depending on the synchrony of the generators (Fang et al. (2020)). In view of this, GFMC converters have attracted the attention of researchers in recent years.

One of the challenges that researchers are facing in relation to GFMC is the impact that internal loops have on system stability. In high and medium power systems, the bandwidth of the controllers is limited by the switching frequency of the switches. That is, the higher the power, the more limited their bandwidth. When studies focus on active power exchange, inertial effect, and transient stability, the internal control design is often neglected due to simplification issues that can lead to system instability (Liu et al. (2015)).

In (D'Arco et al., 2014), it is demonstrated how the sensitivity parameters of the eigenvalues of a linearized small-signal system model can be used systematically to identify controller configurations in order to improve the dynamic response of a given system. The authors take

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into account that conventional control designs for internal loops do not guarantee system stability. These methods are defined by using simplifications and approximations justified by the decoupling of the loops, that is, considering that the voltage loop is much slower than the current loop. In view of this, an algorithm is proposed that uses sensitivity analysis to adjust the gains of controllers that were initially designed by the conventional method, that is, a redesign is made for the controller gains.

In (Qoria et al., 2018), the author analyzes the GMFC system connected to the grid and connected to a resistive load. The author realizes, through simulation, that the system connected to the grid is unstable. In addition to this analysis, the state space model of the complete system was developed, and the eigenvalues were observed. It was proven that they had eigenvalues with a positive real part, confirming what the simulation had predicted. And, to deal with this instability, a method for adjusting the controller gains was developed based on the sensitivity analysis of the eigenvalue parameters of the complete system, showing that the conventional design method for the internal loops can lead the system to instability.

The dynamics of the internal and external control loops are also discussed in (Deng et al., 2022) which evaluates the system connected to the grid and in an autonomous manner. This analysis shows that the dynamics of the internal loop are slower when the converter is connected to the grid. Therefore, a high-pass filter in feedback with the inductor current is proposed to improve the dynamics of the system when connected to the grid. In (Hammouda et al., 2023), the article focuses on the modeling and design of the internal loop controllers of the system in dq0 coordinates. The voltage and current control circuits are implemented based on three PI controllers for the forward, quadrature and DC components. The modeling of the system under study considers the converter connected to an LC filter. The design of the internal loops is done considering simplifications and disregarding the influence of the PWM delay and the current loop on the voltage control design. Through simulation in Matlab/Simulink, it shows the behavior of the designed system. However, the author does not show whether there is in fact stability in the system.

Based on the literature, it can be identified that the designs of the internal loop of the GFMC are complex and many authors resort to simplifications and approximations to facilitate the calculation of control gains, but it is evident that these design simplifications are detrimental to the stability of the system. Given the above, this article proposes a design method for the internal loops of the network-forming converter in an unconventional way, that is, without considering simplifications and thus ensuring the stability of the system connected to the grid. To evaluate the method, a system stability study was carried out based on the complete state-space model developed by Pogaku et al. (2007). In addition, system simulations are performed on the Matlab/Simulink software to analyze the system performance and a Hardware in the loop simulation is also performed using the OP4500 platform to evaluate the system performance in real time.

This paper is organized as follows: Section 2 presents the modeling of the network-forming converter. Section 3 presents the design of the system control loops and the analytical formulation of the complete system. Section 4 presents an analysis of the performance of the inner-loop controllers. Section 5 presents the simulation results in Matlab/Simulink, and Section 6 presents the results obtained on the OP4500 real-time platform with HIL. The conclusions are stated in Section 7.

2. MODELING OF THE NETWORK-FORMING CONVERTER

According to Fig. 1, the state variables that represent the system are, respectively, the converter current i_1 through the inductor $L_1 = 2\ mH$, the voltage across the capacitor V_c over the capacitor $C_f = 15\ uF$ and the current i_2 through the inductance $L_2 = 1\ mH$. Knowing that $R_1 = 0.1\ \Omega$ and $R_2 = 0.2\ \Omega$..

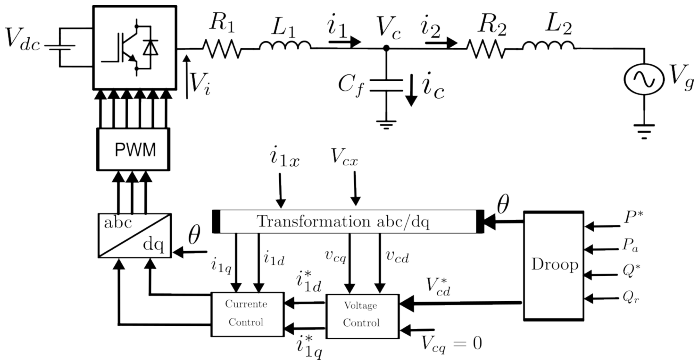

Figure 1. Grid-connected grid-forming converter.

The dynamic equations of the system are presented below:

$$\begin{aligned} V_i - V_c &= L_1 \frac{di_1}{dt} + R_1 i_1 \\ i_1 - i_2 &= C_f \frac{dV_c}{dt} \\ V_c - V_g &= L_g \frac{di_2}{dt} + R_2 i_2 \end{aligned} \tag{1}$$

Considering the transformation of the reference abc to dq, and thus assuming that the three-phase system is symmetric, the dynamic model of the LCL-filtered CFT can be obtained in the dq frame as follows:

$$\begin{aligned} V_{id} - V_{cd} &= L_1 \dot{i_{1d}} + R_1 i_{1d} - L_1 w_0 i_{1q} \\ V_{iq} - V_{cq} &= L_1 \dot{i_{1q}} + R_1 i_{1q} + L_1 w_0 i_{1d} \end{aligned} \tag{2}$$

$$\begin{aligned} i_{1d} - i_{2d} &= C_f \dot{V_{cd}} - C_f w_0 V_{cq} \\ i_{1q} - i_{2q} &= C_f \dot{V_{cq}} + C_f w_0 V_{cd} \end{aligned} \tag{3}$$

$$\begin{aligned} V_{cd} - V_{id} &= L_s \dot{i_{2d}} + R_2 i_{2d} - L_2 w_0 i_{2q} \\ V_{cq} - V_{iq} &= L_s \dot{i_{2q}} + R_2 i_{2q} + L_2 w_0 i_{2d} \end{aligned} \tag{4}$$

where ω_o is the angular frequency ($\theta = \int \omega_o dt$) is the phase angle of the output voltage generated by the droop control). Applying the Laplace transform to the equations above, we have:

$$
\begin{aligned}
i_{1d} &= \left[\frac{1}{L_1 s + R_1}\right][V_d - V_{cd} - L_1\omega_o i_{1q}] \\
i_{1q} &= \left[\frac{1}{L_1 s + R_1}\right][V_q - V_{cq} + L_1\omega_o i_{1d}] \\
V_{cd} &= \frac{1}{C_f s}[i_{1d} - i_{2d} - C_f\omega_o V_{cq}] \\
V_{cq} &= \frac{1}{C_f s}[i_{1q} - i_{2q} + C_f\omega_o V_{cd}] \\
i_{2d} &= \left[\frac{1}{L_2 s + R_2}\right][V_d - V_{cd} - L_2\omega_o i_{2q}] \\
i_{2q} &= \left[\frac{1}{L_2 s + R_2}\right][V_q - V_{cq} + L_2\omega_o i_{1q}]
\end{aligned} \tag{5}
$$

Figure 2 illustrates the diagram of the internal control loops with the compensation and external terms of the network-forming converter. For the design of the internal control loops, it is considered that these terms are compensated.

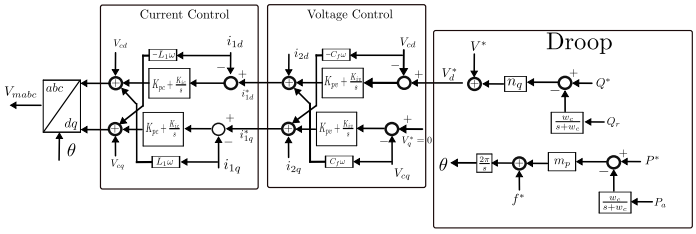

Figure 2. Diagrama malha interna e externa.

3. CASCADE CONTROL LOOP DESIGN

The control of the grid-forming converter consists of two parts: one is the Droop forming block that corresponds to the external loop and the other is the internal loop that has the voltage and current cascade control. The method for calculating the controller gains takes into account the dynamics of the entire system without making simplifications, as in the articles cited in the introduction, that is, for the current loop it takes into account the PWM delay and for voltage control it takes into account the dynamics of the current control.

3.1 External Loop (Droop)

The basic idea of droop control is to emulate the behavior of a synchronous generator. Using the theory of the two d-q axes, the injection of active and reactive power, P_a and Q_r, the following expressions can be obtained:

$$
\begin{aligned}
P_a &= V_{cd} i_{2d} + V_{cq} i_{2q} \\
Q_r &= V_{cd} i_{2q} - V_{cq} i_{2d}
\end{aligned} \tag{6}
$$

To ensure good dynamic decoupling between the outer loop and the inner loop, a filter is added to the measured active and reactive power, where ω_c is the cutoff frequency of the filter.

$$
P_f = \frac{w_c}{w_c + s} P_a \quad Q_f = \frac{w_c}{w_c + s} Q_r \tag{7}
$$

$$
m_p = \frac{f_{max} - f_{min}}{P_{max}} \quad n_q = \frac{V_{max} - V_{min}}{Q_{max}} \tag{8}
$$

Using (6)-(8), it can be deduced that

$$
f = f^* + m_p(P^* - P) \tag{9}
$$

and

$$
v_d^* = V^* + n_q(Q^* - Q). \tag{10}
$$

In Figure 3 the block diagram of the external loop with Droop control is illustrated.

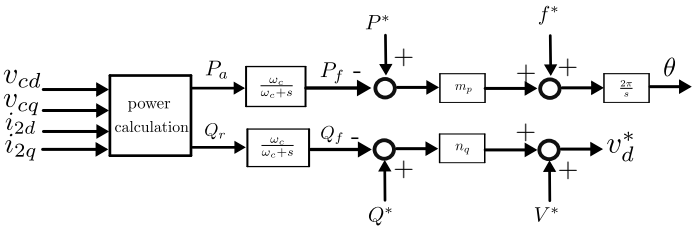

Figure 3. Outer loop diagram (droop).

The calculated values for mp and nq are 3×10^{-4} and 1×10^{-6}. Figure 4 illustrates the value of θ varying from 0 to 2π at a frequency of 60 Hz (f_{ref}). Furthermore, V_{dref} is the reference voltage for the voltage grid varying from 250 V to 300 V. Figure 5 shows the system power, which is maintained at 5000 W.

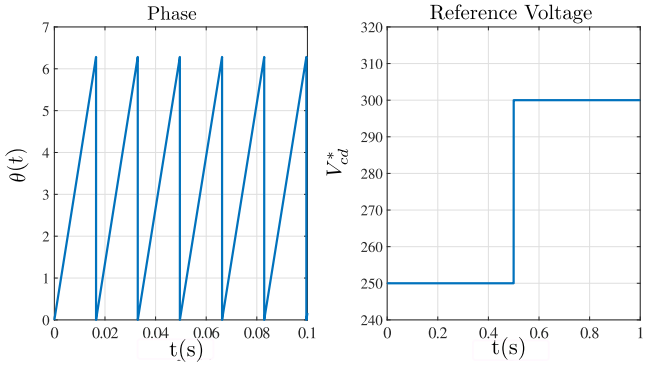

Figure 4. Variation of $\theta(t)$ from 0 to 2π and reference voltage $v_{dref}(t)$ from 250 to 300 V.

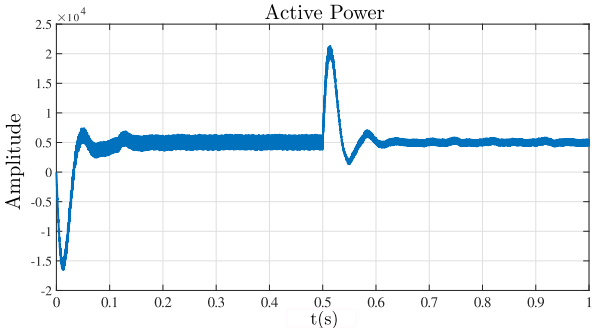

Figure 5. Active power.

3.2 Current Control Loop

Based on the equations of the inductor L_1 and the capacitor C_f in (5), one can construct the block diagram for the design of the voltage and current controllers. The current control is divided into 3 transfer functions which are: the PI controller, the PWM delay function and the plant corresponding to the inductor L_1, illustrated in Figure 6.

Where K_{pc}, K_{ic} and f_{sw} are the PI controller gains and switching frequency, respectively. Defining the design specifications as: maximum overshoot - $M_p \leq 8\%$, bandwidth

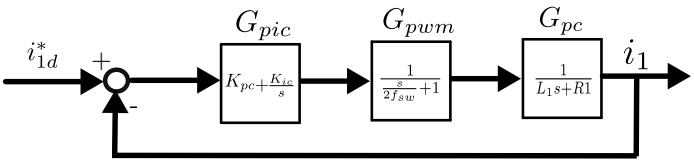

Figure 6. Current control loop

- $BP \leq 800Hz$ and settling time - $t_s \leq 0.001s$. In Figure 7, it illustrates the closed-loop step response of $L(s) = G_{pic} * G_{pwm} * G_{pc}$ and frequency response of $|L(s)|$ and $\angle L(s)$ of the designed control, it can be observed that the design specifications were met. Furthermore, the analytical equations for each d and q axis of the current control are:

$$\frac{d\Psi_d}{dt} = i_{1d}^* - i_{1d}, \quad \frac{d\Psi_q}{dt} = i_{1q}^* - i_{1q}, \tag{11}$$

$$\begin{aligned} V_{dref} &= -\omega_o L_f i_{1q} + K_{pc}\left(i_{1d}^* - i_{1d}\right) + K_{ic}\Psi_d, \\ V_{qref} &= \omega_o L_f i_{1d} + K_{pc}\left(i_{1q}^* - i_{1q}\right) + K_{ic}\Psi_q. \end{aligned} \tag{12}$$

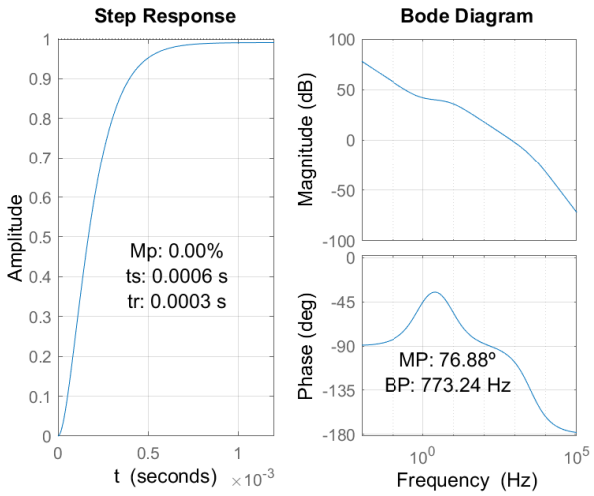

Figure 7. Step and frequency response with $ts = 6\times10^{-4}$ s, $M_p = 0\%$, $BP = 773.24$ Hz

3.3 Voltage Control Loop

Voltage control has 3 transfer functions which are: the PI controller, the closed loop of the current control and the plant corresponding to the capacitor C_f. Knowing that Hc is the closed loop function of the current control. In Figure 8 the block diagram of the voltage control is illustrated.

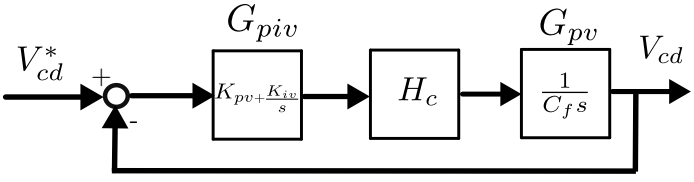

Figure 8. Voltage Control Loop

Where K_{pv}, K_{iv}, H_v are respectively the gains of the PI controller and the closed-loop function of the current control. The design specifications for the voltage control are: $M_p \leq 5\%$, $t_s \leq 0.005$ s and $BP \leq 500$ Hz. Figure 9 illustrates the closed-loop step response of $L(s) = G_{piv} * H_c * G_{pv}$ and frequency response of $|L(s)|$ and $\angle L(s)$ and it can be observed that the specifications were met. The d- and q-axis equations are described below.

$$\frac{d\Upsilon_d}{dt} = V_{cd}^* - V_{cd}, \quad \frac{d\Upsilon_q}{dt} = V_{cq}^* - V_{cq}, \tag{13}$$

$$\begin{aligned} i_{1dref} &= i_{2d} - \omega_o C_f V_{cq} + K_{pv}\left(V_{cd}^* - V_{cd}\right) + K_{iv}\Upsilon_d, \\ i_{1qref} &= i_{2q} + \omega_o C_f V_{cd} + K_{pv}\left(V_{cq}^* - V_{cq}\right) + K_{iv}\Upsilon_q. \end{aligned} \tag{14}$$

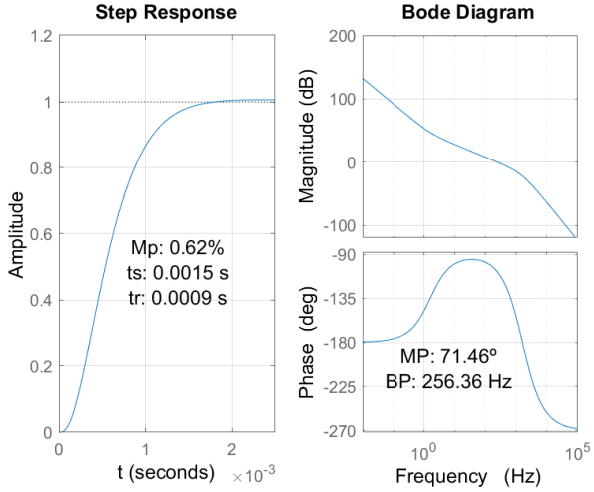

Figure 9. Step and frequency response with $ts = 1.5 \times 10^{-3}$ s, $M_p = 0.62\%$ and $BP = 256.36$ Hz.

Table 1 describes the system specifications and controller gains.

Table 1. System specifications.

Parameter	Value	Parameter	Value
$V_g(RMS)$	380 V	f_o	60 Hz
V_{dc}	600 V	f_{sw}	10 kHz
R_1	0.1 Ω	R_2	0.3 Ω
L_1	2 mH	L_2	1 mH
C_f	15 uF	m_p	3×10^{-4}
w_c	37.7 rad/s	n_q	1×10^{-6}
K_{pc}	9	K_{ic}	500
K_{pv}	0.04	K_{iv}	0.02

3.4 State space model of the complete system

The complete mathematical model is developed by combining the subsystems: LCL filter, external and internal control loops. The model is defined by

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}, \tag{15}$$

sendo

$$\mathbf{x}^T = \left[\delta\theta,\ \delta P,\ \delta Q,\ \delta C_v^{d,q},\ \delta C_c^{d,q},\ \delta i_1^{d,q},\ \delta V_g^{d,q},\ \delta i_2^{d,q}\right] \in \mathbb{R}^{13}$$

e

$$\mathbf{u}^T = \left[V_{cd}^*,\ w^*,\ P^*,\ \delta V_g^{d,q}\right] \in \mathbb{R}^5.$$

The matrix $\mathbf{A}$, through which we can evaluate the stability, and the matrix $\mathbf{B}$ will not be presented due to space restrictions. The equation of state of the complete model is deduced from (2)-(4), (11)-(14), (6)-(7). The 13 states of the complete model are:

- Six states related to the LCL Filter;

- Four states associated with the current and voltage loop controllers;
- Two states related to the filter in P and Q;
- One state related to the angle generated by the droop control,

In Table 2 the eigenvalues obtained from the complete system with negative real parts are described, demonstrating that the system is stable and without the need to redesign the internal loops. Unlike (Qoria et al., 2018) which has a positive real part in its eigenvalues, requiring a redesign of the internal loop controls to avoid instability.

Table 2. Eigenvalues of the state space model of the complete system.

Parameter	Value ($\times 10^4$)	Parameter	Value ($\times 10^4$)
$\lambda_{1,2}$	$-0.4512 \pm 1.0183i$	$\lambda_{3,4}$	$-0.2369 \pm 1.0389i$
$\lambda_{5,6}$	$-0.0358 \pm 0.0000i$	$\lambda_{7,8}$	$-0.0098 \pm 0.0221i$
$\lambda_{9,10}$	$-0.0022 \pm 0.0019i$	$\lambda_{11,12}$	$-0.0014 \pm 0.0000i$
λ_{13}	$-0.0001 + 0.0000i$		

4. PERFORMANCE ANALYSIS OF INNER LOOP CONTROLLERS

In this section, the performance of the designed internal loop controllers will be analyzed. This analysis will be done in two ways, one using the transfer functions as illustrated in Figures 6 and 8 and the second way is to simulate the system using the SimPowerSystem (SPS) library of Matlab/Simulink. As a comparison test, reference signals are applied to both controllers and thus the tracking performance of both is analyzed. Figures 10 and 11 illustrate the tracking of the current control to the established reference from 5 A to 10 A. It is evident that the control is capable of tracking in both simulation conditions.

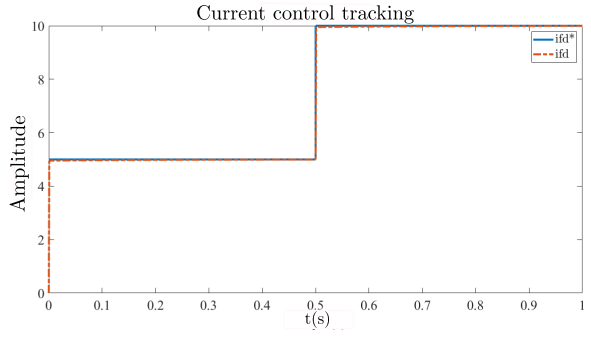

Figure 10. Current control tracking.

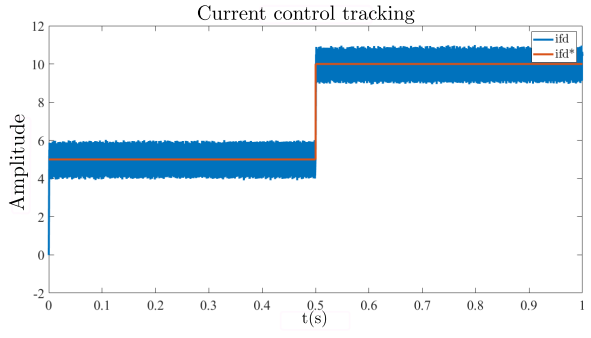

Figure 11. Current control tracking.

Figures 12 and 13 illustrate the tracking of the voltage control at the given step from 250 V to 300 V. It can be seen that in both situations the control is capable of tracking the reference. Note also that there is a difference between the response signals obtained in the figures, since in the simulation of Figures 11 and 13 there is the presence of the converter, LCL filter and PWM that switches at a frequency of 10 kHz. Given this, it can be seen that the response has an associated high frequency ripple.

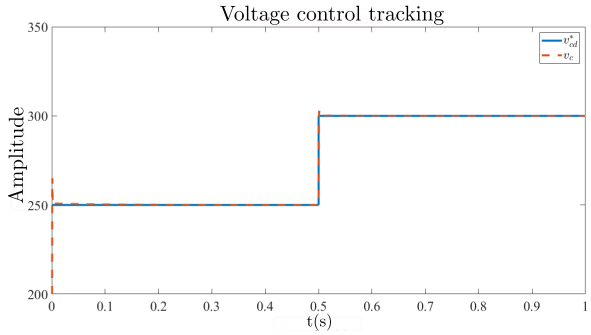

Figure 12. Voltage control tracking.

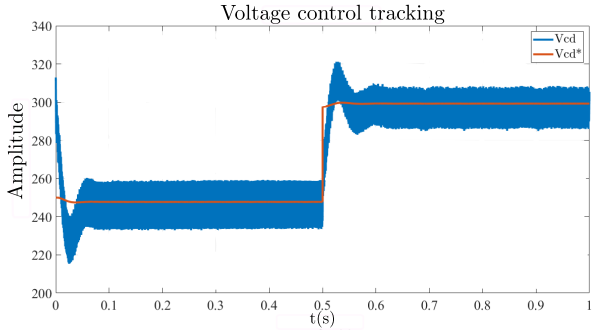

Figure 13. Voltage control tracking.

5. SIMULATION IN MATLAB/SIMULINK

This section addresses the simulation of the grid-connected converter with the presence of the external droop loop in Matlab/Simulink. As a first analysis, a step was given in the reference voltage delivered by the "Droop" control from a voltage of 250 V to 300 V and an active reference power of 5000 W.

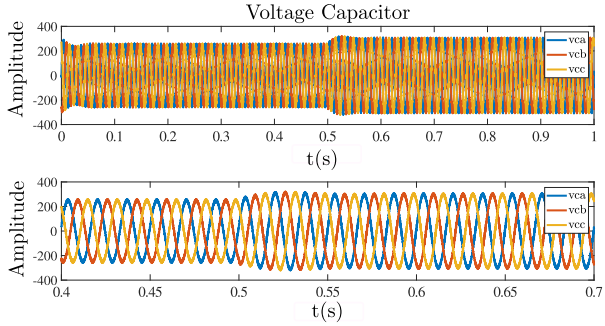

Figure 14. Voltage across the capacitor $V_c(t)$. The lower graph shows a zoom in on the section $0.4s \leq t \leq 0.7s$.

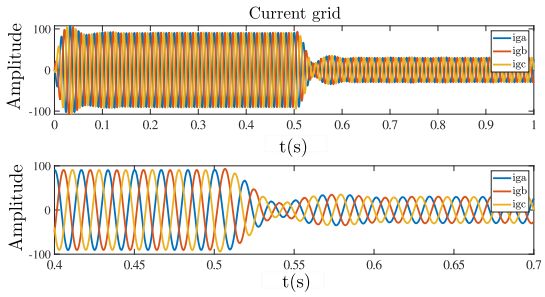

Figure 15. Current $i_2(t)$. The lower graph shows a zoom in on the segment $0.4s \leq t \leq 0.7s$.

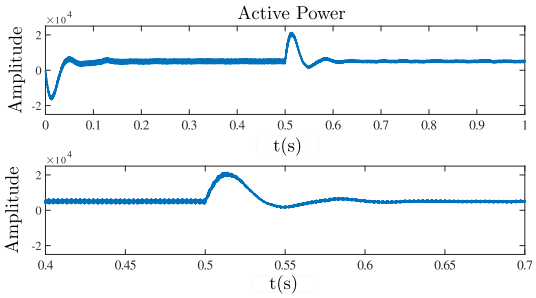

Figure 16. Active power $P(t)$. The lower graph shows a zoom in on the segment $0.4s \leq t \leq 0.7s$.

Figures 14, 15 and 16 illustrate the voltage, current and power after a step in the reference voltage V_{cd}^* (droop). Then a step in the power is given from 0 to 5000 W. What can be observed is that the voltage remained constant, the power goes from 0 to 5000 W and the current follows the power. These responses are illustrated in Figures 17, 18 and 19.

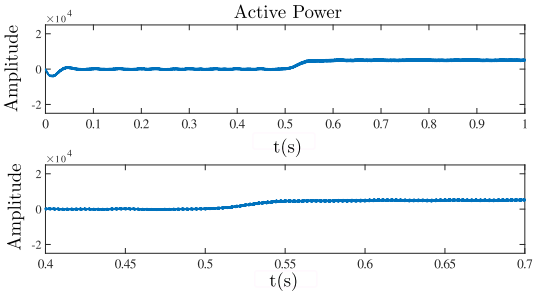

Figure 17. Active power $P(t)$. The lower graph shows a zoom in on the segment $0.4s \leq t \leq 0.7s$.

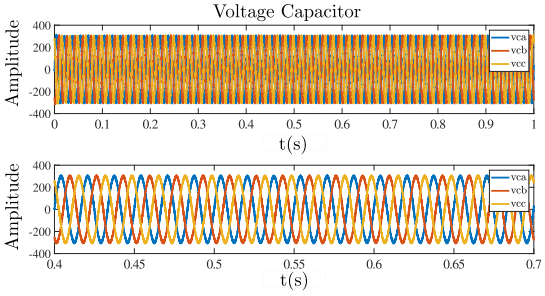

Figure 18. Voltage across the capacitor $V_c(t)$. The lower graph shows a zoom in on the section $0.4s \leq t \leq 0.7s$.

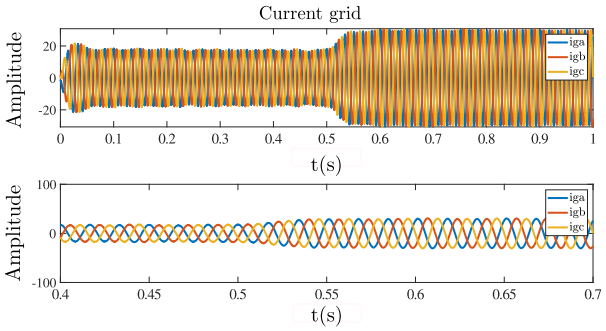

Figure 19. Current in network $i_2(t)$. The lower graph shows a zoom in on the segment $0.4s \leq t \leq 0.7s$.

6. HIL RESULTS - OP4500

This section presents the results of the real-time simulation with the OP4500 in Hardware in the Loop. The objective of this section is to show the behavior of the designed system from the perspective of a real-time simulation and to observe whether the system behavior corresponds to the system simulated in Matlab/Simulink. The same analysis tests that were performed in the previous section with variation of the reference voltage and active power delivered by the droop control are repeated in order to evaluate whether the performance is maintained for the designed internal loops.

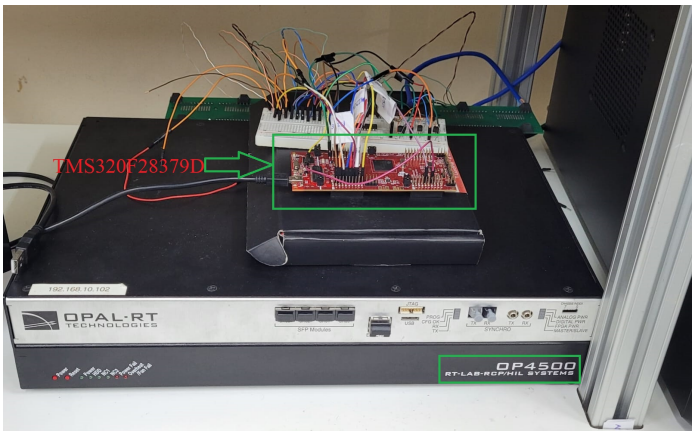

Figure 20. Setup for HIL with TMS320F28379D.

Figure 20 illustrates the connection between the DSP board and the OP4500. The OP4500 is a real-time simulation system developed by Opal-RT Technologies. It is designed to test and validate control and protection systems in real-time environments, especially in power system applications, power electronics, and hardware-in-the-loop (HIL) simulations. Through HIL, the OP4500 has the ability to integrate physical controllers into the simulation system, and thus be able to test controllers before they are deployed in the field, reducing risks and costs associated with design errors. The DSP is a specialized hardware designed to perform digital signal processing efficiently. It has a microprocessor that quickly performs complex mathematical calculations, which is essential in applications that perform signal processing in real time. In this work, the Texas Instruments DSP, named TMS320F28379D, is used. To perform a simulation in HIL, it is necessary to discretize the entire control system, which consists of the internal and

external loops, the PWM, and the abc/dq transformations of the designed system. The Tustin method was used to discretize the PI controllers (Buso and Mattavelli (2015)) with a sampling time of $T_s = 100\ us$. See below the Tustin formula for the discretization.

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \tag{16}$$

The system is implemented in C language in the software provided by the DSP manufacturer, Code composer studio. Figure 21 illustrates the idea used to execute the HIL. Note that the system within the green outline is the power circuit located in the OP4500 and is composed of the converter, LCL filter and the network. Opal-RT provides a library with Simulink that provides useful components for real-time simulation. For the simulation of this work, the RT-Lab tools integrated with the Matlab SPS were used and the calculation step used in the OP4500 was $30us$. The red outline illustrates the control system formed by the PWM, internal and external control loops and the abc/dq transformations that are discretized and implemented in the DSP.

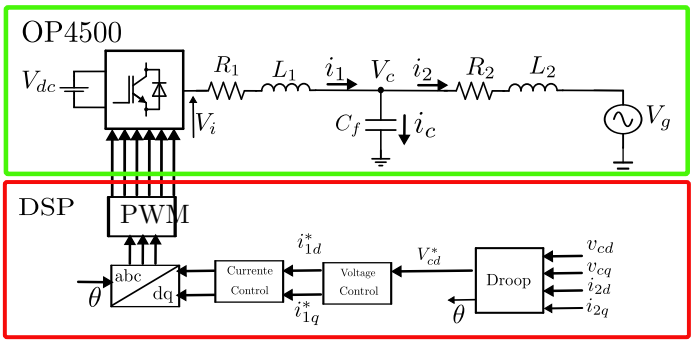

Figure 21. Architecture used in testing with the DSP and the OP4500.

For a first analysis, a reference step in the voltage V^*_{cd} of the forming block (droop) was configured from 250 to 300 V and then from 250 to 300 V and a power P^* of 5000 W to verify if the real-time system is capable of tracking and having the same performance seen in the simulation made in Matlab/Simulink. See in Figure 22 that in channel 1 (yellow) is the current signal of the inductor L1, in channel 2 (green) is the voltage signal in the capacitor V_c controlled by the voltage control and in channel 3 (purple) the active power of the system regulated by the droop control. It can be observed that the same behavior in the Matlab/Simulink simulation is also seen in the HIL simulation, that is, the system is capable of tracking the reference and is stable in steady state. It is remarkable to observe that when there is a voltage step increasing from 250 to 300 V or going from 300 to 250 V, the current i_1 in the inductor L1 decreases and increases, respectively, to keep the power P^* constant. Recall that the measured signals were normalized and sent to the oscilloscope by a constraint on the output voltage of the OP4500.

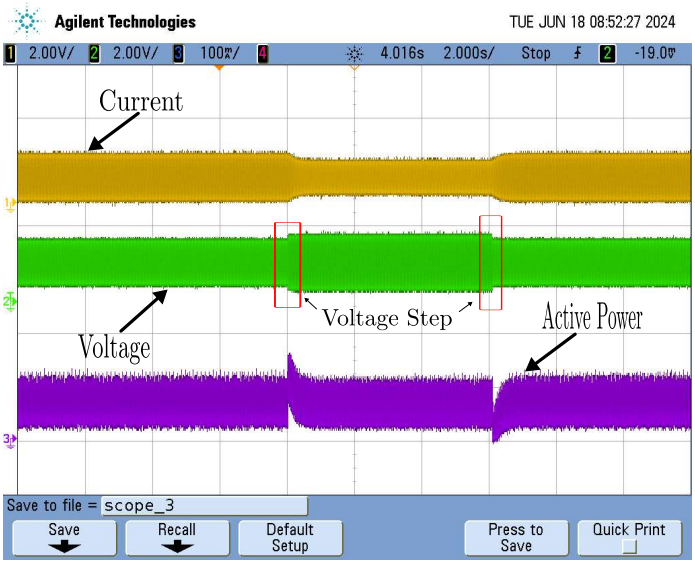

Figure 22. Real-time simulation result.

The second analysis was performed by giving an active power step P^* from 5000 to 0 W and then from 0 to 5000 W in the external loop, in the same way as performed in the previous section. Figure 23 illustrates the response of the HIL system to the step. As expected, the voltage across the capacitor V_c remains constant and the current i_1 in the inductor L1 changes with the step. In a decreasing step from 5000 to 0 W the current decreases and in the increasing step from 0 to 5000 W the current increases and stabilizes to deliver the injected power to the system. Thus confirming the results that the designed system is stable and if placed in a field system it will probably work.

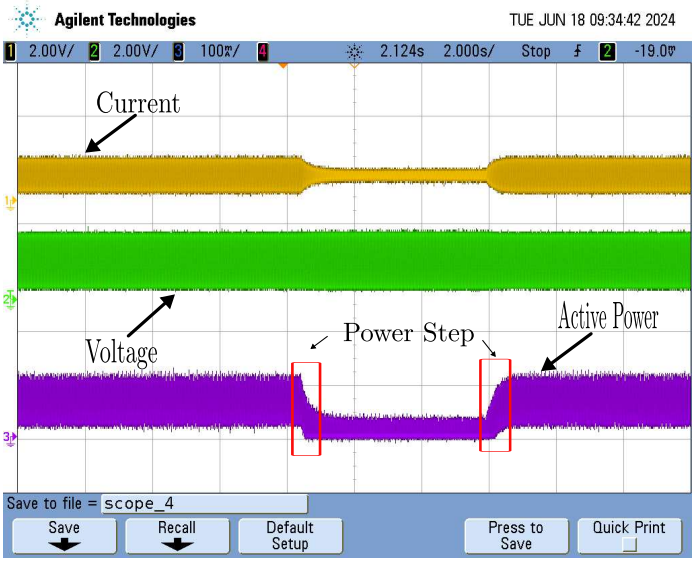

Figure 23. Real-time simulation result.

7. CONCLUSION

This paper presents the modeling and design of the internal and external loops of the grid-forming inverter. The proposed method was developed to design the internal loop controllers, taking into account the influence of the PWM and the current loop on the design of the voltage

loop gains. Then, the state space equation of the complete system was developed to verify the stability of the system, and it was possible to verify that the eigenvalues of the system had a negative real part, thus proving the stability of the system. Therefore, it is not necessary to redesign the controllers as was done by the articles cited in the introduction. In addition, simulations were performed using the transfer functions and the SPS library of Matlab/Simulink to analyze the performance of the designed controllers, and it was possible to verify that in both cases the performance of the controllers follows the reference. In another analysis, the complete system was used in Simulink to verify the performance of the system by observing the system response to the step in the system reference voltage and the reference power and, as expected, in both cases the system maintained its performance. Finally, the system was implemented in the OP4500 to perform the HIL and verify if the system would have the same performance as in the previous tests. For this, it was necessary to discretize the control loops using the Tustin method and use the sampling time of $T_s = 100\ us$. And so, the power circuit was built in the OP4500. The discretized system was implemented in C language on TMS320F28379D and executed in real time on OP4500. It was possible to observe that for the same tests performed in Matlab/Simulink, the system obtained the same results. Therefore, the designed converter implemented in a real environment has a great chance of working. For future work, new analysis is being done, such as exchanging the droop strategy for the dVOC strategy and analyzing the behavior of the internal loops under this new dynamic. Another study is to connect the network-forming converter to a system of n buses to know the impact of this system on the internal loops and finally develop an optimization algorithm to reduce the error of the internal loop controllers by finding the optimal gain values.

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