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Timing Analysis in Pid Controller Using Data and Clock Load

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TIMING ANALYSIS IN PID CONTROLLER USING DATA AND CLOCK LOAD

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Abstract

Proportional-Integral-Derivative (PID) control is the most commonly used control algorithm in industries and has been universally accepted in industrial control, like for industries such as chemical, petrochemical, robotics etc. The popularity of PID controllers is due to the fact that they are low cost, easy to maintain and also gives robust performance in a wide range of operating conditions. In order to improve the performance of the PID controller, Razor flip flops are used to detect and correct timing errors on critical path. In this proposed work, novel Flip Flop called Razor Clock Gated Flip Flop (RCGFF) by using Pulse-Triggered Flip-Flop is introduced. The designed circuit is used to reduce the timing error and increasing the robustness in integrated sequential circuits. RCGFF is mainly contributing to high-precision, high-speed, power reduction in static and average power consumption in PID controller. This technique is suitable for low power and data communication in PID controller. Results are validated by simulations, 74% of power reduction occurs compare to conventional design, by using IBM 130 nm with 1.8 supply voltage. The proposed RCGFF is compared with previous work in terms of power consumption, Power Delay Product (PDP), time delay and area.

Keywords: Proportional-Integral-Derivative (PID) controller, Pulse-Triggered Flip-Flop, Razor and Timing error

I. INTRODUCTION

Most commonly used controllers in the process control industries are PID [1]. The main reason for PID being used is its remarkable effectiveness, relatively explicable structure and simplicity of implementation in practice by process and control engineers [2]. For the last two decades, the attention is subsequently focused on the PID controllers using different high-performance active building blocks such as, Operational Transconductance Amplifiers (OTAs) [3-4], Current Feedback op-Amp (CFAs) [5-6], second generation Current Conveyors (CCIIs) [7], second generation Current Controlled Current Conveyors (CCCIIs), and Current Differencing Buffered Amplifiers (CDBAs) [8].

The PID controller is probably the most widely-used type of feedback controller [9]. PID stands for Proportional-Integral Derivative, referring to the three terms operating on the error signal to produce a

control signal. By tuning the three parameters in the PID controller algorithm, the controller can provide control action designed for specific process requirements. The response of the controller can be described in terms of the responsiveness of the controller to an error, the degree to which the controller overshoots the set point, and the degree of system oscillation. The system process is an analog signal to obtain the output by ADC. In this, both ADC and DAC are introducing the error, delay, and data loss. The timing error is a type of error which causes the unnecessary delays in the execution of the program. The timing error causes because of scaling in CMOS technology, increase of process variations, due to power supply minimization and due to increasing complexity of modern ICs. There are various techniques used for an error detection and correction. In this proposed work, the PID is implemented with Razor system to correct the timing error.

Razor Flip-flop is to mainly use to operate the circuit at sub-critical voltage and tune the operating voltage by monitoring the error rate [10-12]. Razor is a circuit-level technique which is used to detect and correct timing errors on critical path. In this proposed work, Razor Clock gated Flip Flop (R- CGFF) for reduce the timing error in every bit and achieve maximum power reduction in the PID controller system.

II. RAZOR BASED DESIGN

Razor flip-flop is mainly used to detect and correct the timing errors on critical path and to purposely operate the circuit at sub-critical voltage and tune the operating voltage by monitoring the error rate [13]. This eliminates the need for conservative voltage margins. It consists of main flip-flop and shadow flip-flop which is controlled by a delayed clock is shown in Figure 1. Timing errors can be detected by comparing the data from the main flip-flop with shadow flip-flop [14-15]. If an error is detected, it is corrected by restoring the data from the shadow latch to the main flip-flop. It allows the timing guard band to be eliminated or to be reduced. Timing errors are detected and corrected by on-chip circuits when they occur. If any flip-flop in a stage receives a signal with critical path delay, then all the flip-flops in that stage must be replaced by RFFs.

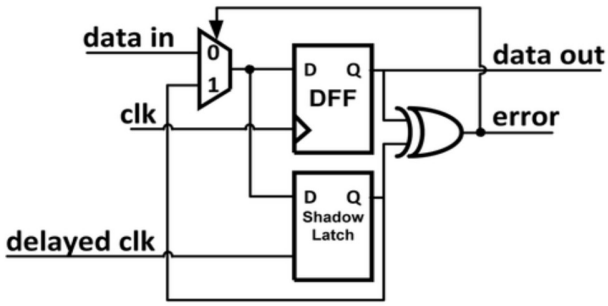

Figure.1 Razor Flip-flop

In razor Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master-slave- based FF in the applications of high-speed operations. In Razor FF, P-FF design is classified into implicit or explicit. In an implicit pulse generated are built in the latch. The pulse generated externally to latch is explicit. The power efficiency of the implicit type is higher than the explicit pulse generator. Due to this reason, the Razor FF is designed using conventional Implicit-Type P-FF, such as SDFF (Semi-Dynamic Flip-Flop), HDFF (Hybrid Latch Flip-Flop), and DDFF (Dynamic data Flip-flop).

2.1 Semi-Dynamic Flip-Flop (SDFF)

Semi-Dynamic Flip-Flop has been used in high performance applications because of its small delay, logic embedding feature and simple topology. The circuit is constructed with dynamic input stage with static operation hence it is called as semi-dynamic. The operation of the circuit is defined with precharge and the evaluation region. During the falling edge of clock, the flip-flop enters the precharge phase. When the clock rises, the flip flop enters evaluation phase.

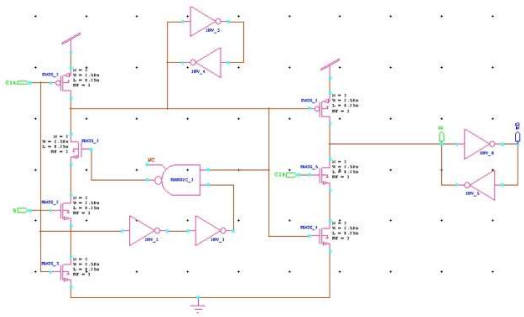

Figure 2. Semi-Dynamic Flip-Flop

In SDFF clock signal is input is given to P1, N3 and inverter I1 and I2 are generated the pulse delay to the conditional NAND gate is shown in fig 2. During clock rising edge N3 will turn ON. N3 node is discharge when data D remains low switching activity of transistor which leads to more power dissipation.

2.2 Hybrid Latch Flip-Flop (HDFF)

HLFF samples the data on one edge of the clock and eliminates the obstruction (delay) of data flow on the reverse edge. HLFF is mainly aimed to design the substantial reduction in latch latency and clock load. The basic operation is similar to latch because it delivers a soft clock edge which allows for the stack passing and minimizing the effects of clock skew on cycle time. This cycle time is determined by an assimilated one-shot derived from the clock edge.

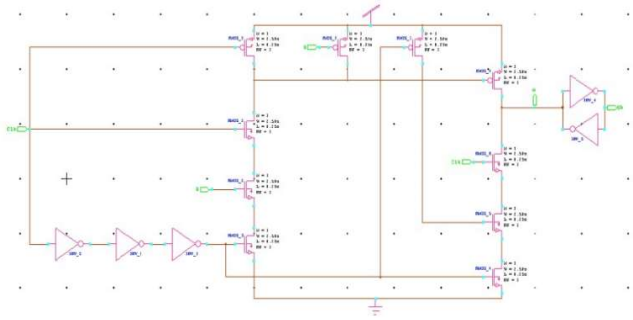

Figure 3 Hybrid Latch Flip-Flop

In HDFF Delay clock signal is generator by inverters I1-I3. Flip-flop output signal Q is maintained high with respect to the pull-up transistor P3 with the gated input clock signal. During data “0” to “1” transitions, Q node is not pre-discharged. Larger transistors N1 and N4 are required to enhance the discharging capability.

2.3 Dynamic Data Flip-Flop (DDFF)

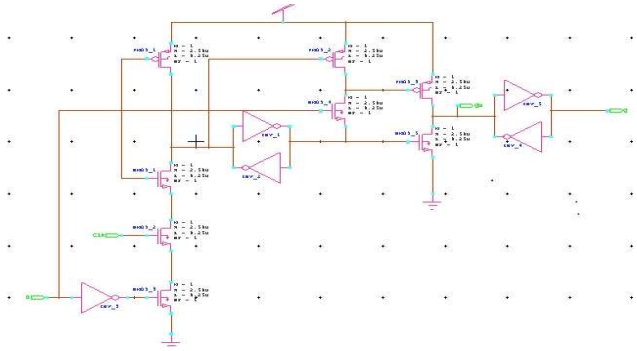

Figure 4 Dynamic Data Flip-Flop

In figure 4 DDFF are designed by Keeper logic method. The feedback inverteris weak pull up in PMOS_2 and NMOS_2 are connected to the load capacitance to keeper logic gate, hence there is no discharging in voltage swing and no properly pull-down this ensure the extra circuitry.

2.4 Clocked CMOS Flip-Flop (CCMOS)

To overcome the drawback of the data float in keeper logic at node INV1 and INV2,

clocked CMOS was proposed. In CCMOS voltage scaling are controlled by data input of both pull-up and pull-down network. Clock and clock bar inputs are controls the data path voltage. In the drain node of PMOS2 and NMOS2 is feedback to the strong pull-down and pull up network.

In the pull-down, NMOS6 and PMOS5 are voltage swing controlled with respect to the I1. Based on Clock and clock bar swing voltage are pull down in transistor NMOS9 and PMOS5. This implies the strong discharging in load capacitance at the drain node of N9 and P5. To ensure datapath in a pull up in properly voltage scaling is controlled by P1 and N4 with respect to gated input I1.P4 and N1 are clocked controlled and ensure the powerful pull-down, with wider of I2 and I3 inverters and longer delay from I1 to I3 pulse width are properly discharge in load capacitance.

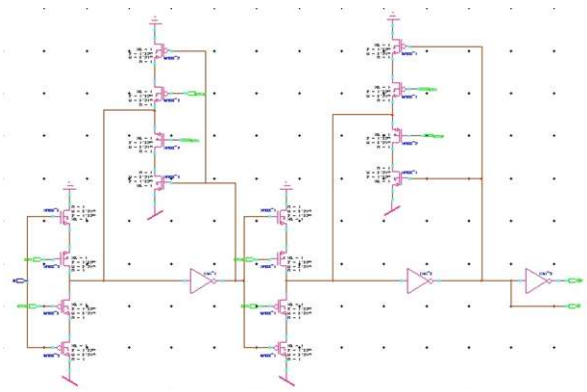

Figure 5 Clocked CMOS Flip-Flop

Clocked CMOS circuits, which adopt gradually rising and falling power-clock, can result in a considerable energy saving. However, the demand that the output signal should track the power-clock's gradually rising and falling behaviour during charging and discharging makes the circuit design even difficult.

III Proposed Razor CGFF with PID controller

The proposed work designed a novel Razor Clock Gated Flip Flop (RCGFF) by using Pulse-Triggered Flip-Flop to reduce the timing error in PID controller.

Error detection and correction

In this proposed RCGFF, the delay clock signal is given to shadow flip-flop for detecting the error signal in circuit level. If the combinational logic meets the setup time of the main flip-flop, then the main and delayed flip-flops will latch the same value. In this case, the error signal remains low. If the setup time of the main flip-flop is not met, then the main flip-flop will latch a value that is different from the shadow flip-flop[16].To guarantee that the shadow flip-flop always latches the input data correctly, the input voltage is constrained such that under the worst-case condition, the logic delay does not exceed the shadow flip-flop's setup time. Compare to DDFF, node discharge in RCGFF has huge pull down in each stage of data, this maintains the low switching activity of transistor and low noise capacitance discharge.

In pipeline stage, efficient error detection and correction fails in critical path delay. To meet this clock delay shadow Flip-flop meets the main flip-flop at rising or falling edge data remains the same in both flip-flops. If XOR gate fan out is low error signal are occur and its corrected by shadow flip-flop until XOR gate fan out are high as shown in figure 6.

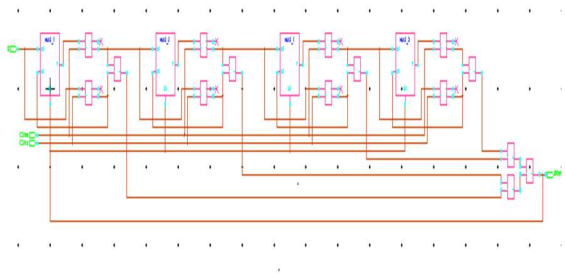

Figure 6 Proposed Razor CGFF

In order to correct the timing error, the PID controller is implemented with Razor system. Design of Proportional Integral Derivative (PID) controllers has received a great deal of attention in the fields of control systems. The PID controller is simple and cheap, and tuning of its parameters is easy. The PID controller circuit designed using Current Conveyor Transconductance Amplifier (CCTA), it consists of capacitors and resistors to match the input voltage as shown in figure 7. Based on Ic1, Ic2 and Ic3 bias current it may operate as P, PI, PD and PID as shown in table 1.

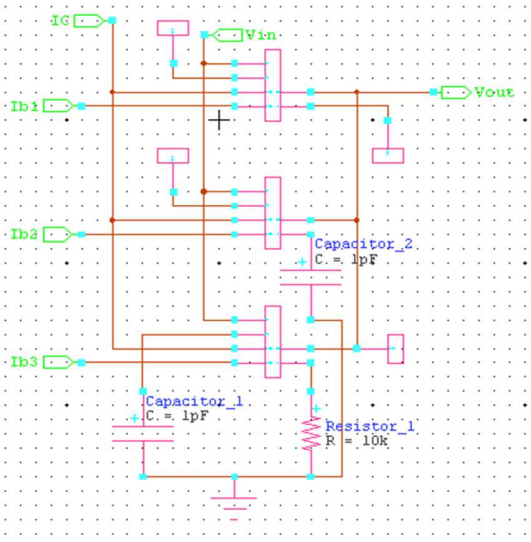

Figure 7 Razor implementation in PID controller

Table. 1 PID Programming

IC1	IC2	IC3	controller
1	0	0	P
0	1	0	I
0	0	1	D
1	1	0	PI
1	0	1	PD
0	1	1	ID
1	1	1	PID

Razor implementation in PID as shown in figure 7. The structure consists of DVS, Razor II,and PID. To obtain the data loss system Razor function compare the data in M-FF and S-FF with respect to the clock signal Clkm (main FF clock) and Clks (shadow FF clock). Clks is a delay signal which is given to razor II. In Razor, both flip-flops meet the same value. Data is passed to the PID controller. If different value shadow FF will correct the value, with respect to clock delay. Based on Ib1, Ib2, Ib3and VIN PID will generate the signal and feedback to the DAC Management. Feedback signal is a nonlinear. Input voltage scaling down in DVS again looped to razor II. It will repeat until linear feedback. The schematic diagram of Razor implementation in PID controller is shown in figure 8.

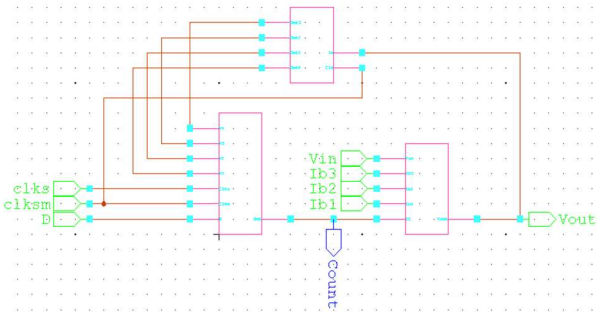

Figure 8. Schematic diagram of Razor implementation in PID controller

IV. EXPERIMENTAL RESULTS

The simulations have been carried out through Tanner EDA tool using 130nm CMOS parameters. The proposed RCGFF is compared with previous work such as SDFF, HDFF,and Clocked CMOS interms of power consumption, Power Delay Product (PDP), time delay and area. Both convention and proposed Flip-flop are tested in data driving and clock drive. In order to estimate the data power, with and without load to data path are tested in the flip-flop. Total power is defined as the summation of data driving power, the clock driving power and internal power. The simulation parameters are represented in table 2.

Table 2: Simulation Parameters

Device Technology	130nm CMOS technology
C1 , C2	100 pF
VDD	1.2 V
-VSS	1.2 V
Ib1	55 µA
Ib2	24 µA
Ib3	30 µA
KP	1
TI	0.43u10-6 s
TD	1u10-6 s

The simulated frequency responses of PI controller when the digital signals were IC1= 1, IC2 = 1, IC3 = 0. PD controller when the digital signals were IC1 = 1, IC2 = 0, IC3 = 1. Simulated frequency and phase responses of the proposed PID controller when the digital signals
were IC1 = 1, IC2 = 1, IC3 =1. For logic 1, CCTA used 20 µA for IC1, IC2 and IC3. For logic "0" CCTA used 0A for IC1, IC2 and IC3 logic "0". Table 3 shows the comparison between Convention Flip flops and CCMOS design.

Table 3. comparison of DFF in Pulse mode

Parameter	Data Driving (mw)		
	With load	Without load	Data power
SDFF	1.5239	1.0531	0.4708
HDFF	0.12897	0.0000584	0.1289116
DDFF	0.665337	0.22518	0.440157
C²MOS	0.893957	0.87077	0.023187

Parameter	Clock Driving (mw)		
	With load	Without load	Clk power
SDFF	1.5239	0.7589	0.765
HDFF	0.12897	0.00001316	0.1289568
DDFF	0.665337	0.559771	0.105566
C²MOS	0.893957	0.87077	0.023187

Parameter	Internal power (mw)	Total Power (mw)
SDFF	3.811	5.6291
HDFF	4.6	4.72901524
DDFF	3.523	3.853746
C²MOS	0.87515	1.769107

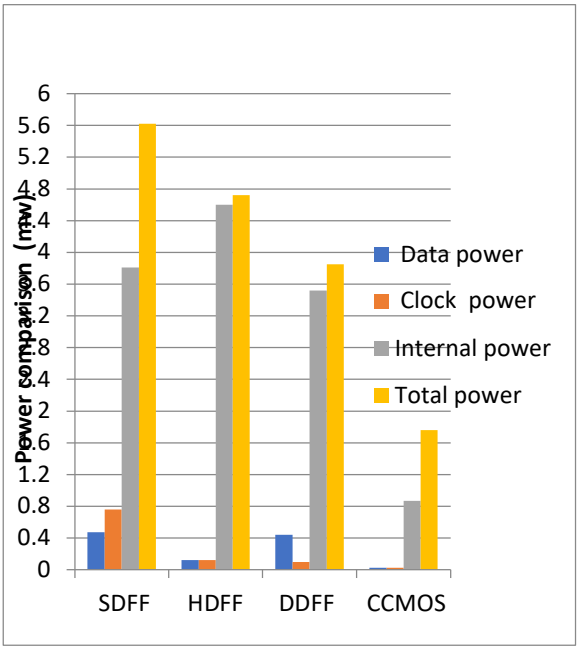

Figure 9. Graphical representation of power comparison for DFF in Pulse mode

Table 4 shows the comparison between convention Flip flops and proposed Clock gating proposed RCGFF design.

Table 4 .Comparison of DFF in Pulse mode

Razor					
Parameter	**SDFF**	**HDFF**	**DDFF**	**CCMOS**	**RCGFF**
Avg power (mw)	15	8.5	7.9	6.4	1.62
Static power (mw)	47.3	11.7	10.3	22.12	3.43
Static current (mA)	26.2778	6.5	5.72	12.28	1.90
PDP (ns)	473	58	51	442	123
Time Delay	6.59 ns	41.9 ns	4.85us	2.45us	4.04ns
operating frequency	100 MHz	100 MHz	100 MHz	100MHz	100 MHz
No of Transistor (area)	295	292	290	294	274

From table 4, the proposed RCGFF is achieves better power consumption, PDP, time delay and area compared with the SDFF, HDFF,and Clocked CMOS. Due to the high power consumption , delay and area the deigned RCGFF is integrated with PID controller for achieving timing error detection. Table 5 shows the comparison of Razor in PID.

Table 5. comparison of Razor in PID

Razor in PID controller					
Parameter	**SDFF**	**HDFF**	**DDFF**	**CCMOS**	**RCGFF**
Avg power (mw)	12	9.23	8.07	4.25	4.00
Static power (mw)	50.8	18.5	8.78	12.44	6.48
Static current (mA)	28.26	10.27	4.87	6.91	3.60
PDP (ns)	254.423	240.666	131.7	311	298.5

Time Delay (us)	10	2.202	21.9	10	10
operating frequency	100 MHz	100 MHz	100 MHz	100MHz	100 MHz
No of Transistor	414	350	348	390	370

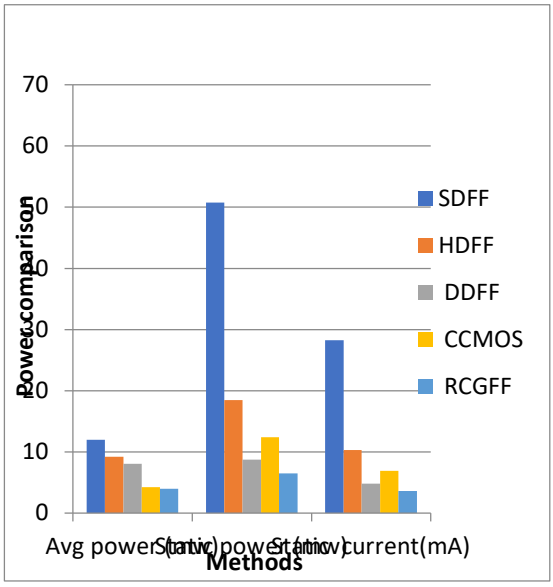

Figure 10. Graphical representation of power comparison for Razor in PID

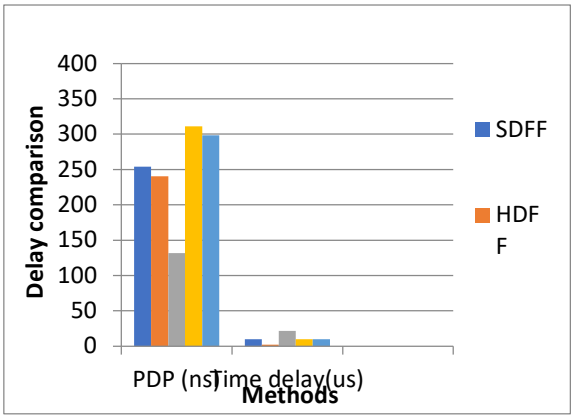

Figure 11. Graphical representation of delay comparison for Razor in PID

Table 6 shows the Error calculation in PID controller with various type of FF Design. The frequency are carried out and controlled on every proportional, integral and derivative term. The combined counters are used to calculate the base frequency f_A in equation 1, and its directly related to the f_P,f_I and f_D. Frequencies cause, the steady-state error. With derivative control, the control signal can become large if the error begins sloping upward, even while the magnitude of the error is still relatively small. This anticipation tends to add damping to the system, thereby decreasing overshoot. The addition of a derivative term, however, has no effect on the steady-state error.

$$Kz = \frac{fz}{fa}, z = P, I, D$$

Proportional Error Signal

$$Kp = \frac{fp}{fa}$$

Integral Error Signal

$$Ki = \frac{fi}{fa}$$

Derivative Error Signal

$$Kd = \frac{fd}{fa}$$

Table 6. Error calculation in PID controller

Parameter	SDFF	HDFF	DDFF	CCMOS	RCGFF
K_p	0.5	0.5	0.5	0.5	0.5
K_i	1.66	4.78	0.384	0.909	0.384
K_d	1	0.37	0.5	0.4	0.4
K_z	0.0316	0.056	0.0138	0.1809	0.01284

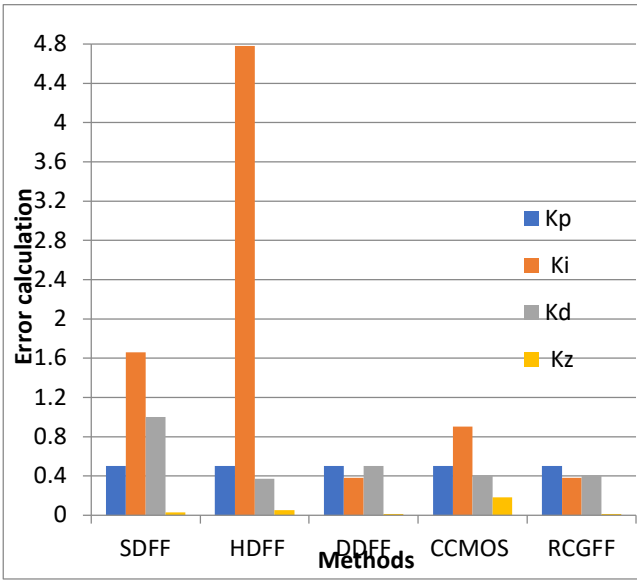

Figure 12. Graphical representation of Error calculation in PID controller

From table 6, the proposed RCGFF is achieves minimum error rate compared with the SDFF, HDFF,DDFF and Clocked CMOS.

V. Conclusion

The proposed work designed a Razor clock gated flip-flop for PID controllers. RCGFF is mainly contributing to high-precision, high-speed, power reduction in static and average power consumption in PID controller. This technique is suitable for low power and data communication in PID controller. The primary advantages of this new structure are low power, low leakage current, and low Timing error. The proposed RCGFF is compared with previous work such as Semi-Dynamic Flip-Flop (SDFF), Dynamic Data Flip-Flop (DDFF), Hybrid Latch Flip-Flop (HDFF) and Clocked CMOS Flip-Flop (CCMOS) in terms of power consumption, Power Delay Product (PDP), time delay and area.

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